





# Dual-T-Type Five-Level Cascaded Multilevel Inverter With Double Voltage Boosting Gain

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**Abstract**—The switched-capacitor-based cascaded multilevel inverters (CMI) have been emerging due to their voltage boosting capability. Unfortunately, they suffer from impulse charging current and nonuniform operation. This article presents a topology termed as dual-T-type five-level CMI to resolve these problems without compromising the desirable voltage boosting characteristic. The main idea is to integrate a half bridge and an inductor to soft charge a capacitor that is connected in series with the dc source. The capacitor enables the voltage gain boosted to two, while the control of eight power switches that constitutes a dual-T structure enables five voltage levels generation. In addition, uniform operation is achieved for cascaded extensions. The operating principle of the proposed topology is analyzed and elaborated. For validation, simulation, and experimental results of a prototype are presented.

**Index Terms**—Cascaded multilevel inverter, dual-T-type topology, soft charging, switched-capacitor, voltage boosting.

## I. INTRODUCTION

IN THE last decades, multilevel inverters have been extensively researched in view of the continuous development of power devices and the fast growing need for emerging applications such as microgrid. The conventional topologies, i.e., neutral-point-clamped inverter, flying capacitor inverter, and cascaded H-bridge (CHB) inverter have been proven as mature solutions for industrial applications [1]–[3]. However, this does not hinder continuous research effort in contributing new promising topologies to offer wider possibilities in multilevel inverter technology [4], [5].

Being one of the most well-established multilevel inverters that has been successfully commercialized, CHB inverter stands out due to its attractive modularity feature. Significant interest

has been garnered in the development of alternative modules in place of H-bridge for improved performance.

To date, various types of cascaded multilevel inverters (CMI) have been proposed in literature. Most of them are based on the concept of switched dc source [6], where each of its isolated dc source is controlled by a half bridge to generate unipolar voltage levels across the dc link [7]. Bipolar output voltage is achieved by controlling an H-bridge connected across the dc link. This topology is therefore termed as multilevel dc-link inverter. In a similar topology in [8], a T-type inverter has been proposed as a replacement for the H-bridge.

In the recent works, considerable attention has been focus on developing cascaded modules by utilizing T-type inverter. An E-type module that combines a T-type inverter, a half bridge, and four additional power switches is presented in [9]. With four asymmetrical dc sources, 13 voltage levels can be generated. A slight modification in [10] can further increase the number of levels to 17 by replacing the half bridge in [9] with a T-type inverter to constitute a two back-to-back T-type inverters structure. Despite not being mentioned in the literature, it is found that the ratio of asymmetrical dc sources is extended from  $2V_{dc}:V_{dc}$  to  $3V_{dc}:V_{dc}$ , which aggravates the power balancing issue. Similar topologies based on back-to-back T-type inverters are also presented in [11] and [12]. The module in [11] can be extended by enclosing more T-type inverters. Alternatively, [12] proposes to extend the module to a switch-ladder structure by connecting more dc sources in series. Optimal design of this topology has validated its lowest power switch count compared to other cascaded modules. While the freewheeling current during dead-time commutation is not taken into account in the design, this topology is suffering from voltage spikes during transition between voltage levels [13].

All the aforementioned modules require the same number of dc sources as that in CHB due to their limited voltage gain. To address this problem, switched-capacitor (SC) based CMI (SC-CMI) are established [14]–[20]. Self-voltage balancing and voltage boosting are two distinctive benefits of SC-CMI. The former is achieved by charging the SCs in parallel with the dc source, while the latter is achieved by discharging the SCs in series with the dc source. However, these advantages come at the expense of the impulse charging current issue, hindering the implementation of this topology in practical applications. In addition, nonuniform operation of SC-CMIs is also a challenge that does not fulfill the modularity characteristic of CMI.

This article proposes a novel CMI topology that resolved the impulse current and nonuniform operation problems of

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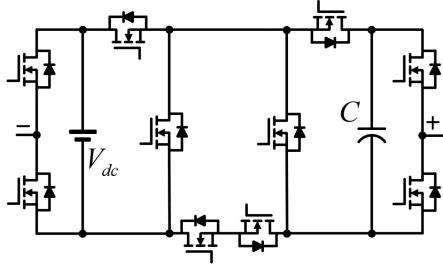


Fig. 1. Five-level switched-capacitor-based cascaded multilevel inverter.

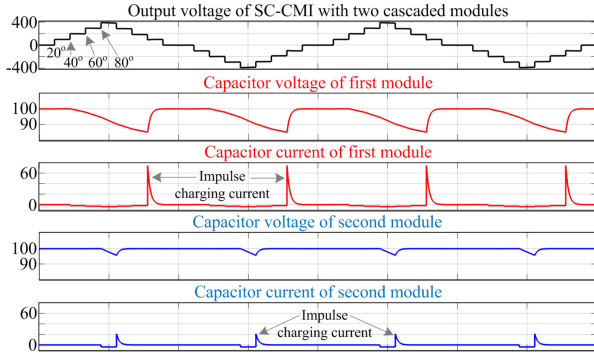


Fig. 2. Simulation results of SC-CMI in Fig. 1 with two cascaded modules.

SC-CMIs while retaining the merits of self-balancing and voltage boosting. The rest of this article is organized as follows. Section II evaluates the problems of SC-CMIs. Section III presents the proposed topology with its analysis and extensions. Section IV discusses the simulation results. Section V presents the experimental results of a prototype. Finally, Section VI draws the conclusion.

## II. PROBLEMS OF SWITCHED-CAPACITOR-BASED CASCADED MULTILEVEL INVERTER

A five-level topology, depicted in Fig. 1, is considered to demonstrate two principal problems faced by a typical SC-CMI. It is a single-stage topology with one SC that is charged to  $V_{dc}$  by connecting it in parallel with the dc source during 0,  $V_{dc}$  and  $-V_{dc}$  levels. Two additional voltage levels are made possible by discharging the SC in series with the dc source. This generates a total of five voltage levels with the attainable maximum voltage level twice of the dc source voltage, thus indicating a voltage gain of two.

Fig. 2 shows the corresponding simulation results of the five-level SC-CMI when a dc source voltage of 100 V and power MOSFETs with ON-resistance of 0.1  $\Omega$  are considered. With two cascaded modules ( $n = 2$ ), it is noted that there are nine apparent symmetrical voltage levels in between 400 and  $-400$  V. The voltage and current of the capacitor in each module, however, reveal the following problems.

### A. Impulse Charging Current

The SC is charged to  $V_{dc}$  by connecting it in parallel with dc source. The difference between  $V_{dc}$  and the SC voltage inevitably leads to the existence of impulse current, which

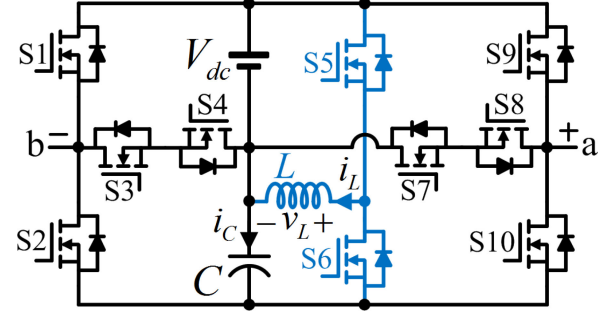


Fig. 3. Proposed DTT-5L-CMI.

reduces the reliability of the electrolytic capacitor as well as the multilevel inverter. Besides, the use of oversized power MOSFETs with extremely high current rating are mandatory to accommodate the impulse current. Note that the magnitude of the impulse current is determined by the ratio of capacitor voltage ripple to the ON resistance of conducting power MOSFETs in charging path.

### B. Nonuniform Operation

Typically, the charging of SC takes place prior to its discharging process, as illustrated in Fig. 2. Considering the case of unity power factor load in Fig. 2, greater voltage levels are generated in the vicinity of the peak load current (i.e., around  $90^\circ$  and  $-270^\circ$  of output voltage) when the SC is discharged. In this instance, exceptionally high-voltage ripples are anticipated. Note that the ripple magnitude of the first module is higher than that in the second module due to their different discharging periods. It is clearly seen that the discharging period for capacitor in the first module is longer than that in the second module, with the former discharges over a span of  $100^\circ$  ( $40^\circ$ – $140^\circ$  and  $220^\circ$ – $320^\circ$ ) while the latter discharges over a span of only  $20^\circ$  ( $80^\circ$ – $100^\circ$  and  $260^\circ$ – $280^\circ$ ). Another observation worth emphasized is the different impulse current magnitudes in both modules, which are attributed to the different voltage ripple as mentioned earlier.

It is now clarified that the SC-CMI sacrifices the modularity property of CMI as components with different ratings are needed in each module. The shortcoming will be further aggravated if higher number of cascaded modules are taken into consideration. This is because the discharging period of the SC between the first module and the last module is elongated. To unify the charging and discharging periods of SC-CMI modules, some special switching strategies are required.

## III. PROPOSED DUAL-T-TYPE FIVE-LEVEL CASCADED MULTILEVEL INVERTER

The topology of the proposed dual-T-type five-level CMI (DTT-5L-CMI) is depicted in Fig. 3. Voltage boosting is achieved by connecting a capacitor  $C$  in series with the input dc source. To prevent the impulse charging current as in the case of SC-CMI, an inductor  $L$  that is controlled by a half bridge (S5 and S6) is integrated in the topology to achieve soft charging. The rest of the switches constitute two T-type inverters for ac voltage generation.

### A. Steady-State Analysis

The switching states of the proposed DTT-5L-CMI are analyzed and summarized in Fig. 4. With capacitor  $C$  charged to  $V_{dc}$ , the maximum voltage level is  $2V_{dc}$ . Five symmetrical voltage levels are generated in between  $2V_{dc}$  and  $-2V_{dc}$ .

Some switches are turned ON despite they are not conducting load current so as to provide a commutation path for the inductive load current during dead time. Taking state [0] as an example, S3 and S8 are two nonconducting switches that are turned ON to cater for the dead-time commutation. Considering the case when there is a voltage level transition from 0 V to  $V_{dc}$ , both S7 and S10 are OFF to prevent short circuit across capacitor  $C$ . Assuming an inductive load with S8 is ON, the negative load current can freewheel through S8 as well as the antiparallel diode of S7. The load voltage will eventually clamped to  $V_{dc}$  during dead time, ensuring smooth transition from 0 V to  $V_{dc}$ . On the other hand, if S8 is OFF, the negative load current is forced to flow through the antiparallel diode of S9. A voltage spike of  $2V_{dc}$  will be generated during dead time, which is highly undesirable. It is therefore important for all the switching states to be design with careful consideration to avoid voltage spike during switch transitions.

For achieving soft charging of capacitor  $C$ , S5 and S6 are controlled complementary with a constant duty cycle of 0.5. Energy is stored temporarily into inductor  $L$  by turning ON S5 before it is discharged to capacitor  $C$  when S6 is switched ON. To reduce cost, S6 can be replaced with a diode. However, active power MOSFET is recommended in view of its bidirectional power flow capability.

The switching states in Fig. 4 shows that switches S1, S2, S5, S6, S9, and S10 each blocks a maximum voltage of  $2V_{dc}$ , while voltage stress on the remaining switches are restricted to  $V_{dc}$ . On the other hand, the current conduction path analyzed in Fig. 4 depicts that the current stress on S5 and S6 are determined by the inductor current, while that on the remaining switches are equal to load current.

### B. Average Capacitor Voltage $V_C$ and Average Inductor Current $I_L$

Fig. 4(f) shows that inductor  $L$  is used to store energy for the first half switching period prior to discharging its energy to capacitor for the remaining period. During steady-state operation, the average voltage of inductor  $L$  is zero. Therefore, the average capacitor voltage  $V_C$  is equal to the dc source voltage

$$V_C = V_{dc}. \quad (1)$$

As inductor  $L$  is operated with a constant duty cycle of 0.5, the average power flowing into capacitor  $C$  is

$$P_{C,in} = 0.5I_L V_{dc} \quad (2)$$

where  $I_L$  represents the average inductor current. To determine the average power flowing out of the capacitor, the load component of capacitor current  $i_{C,Load}$ , depicted in Fig. 5, is considered. Taking the average of the half-wave rectified current waveform, the average current supplied by the capacitor to the load is  $2MV_{max}/\pi R_{Load}$ , where  $M$  indicates the modulation index,  $V_{max}$  indicates the maximum voltage level ( $2V_{dc}$ ), and

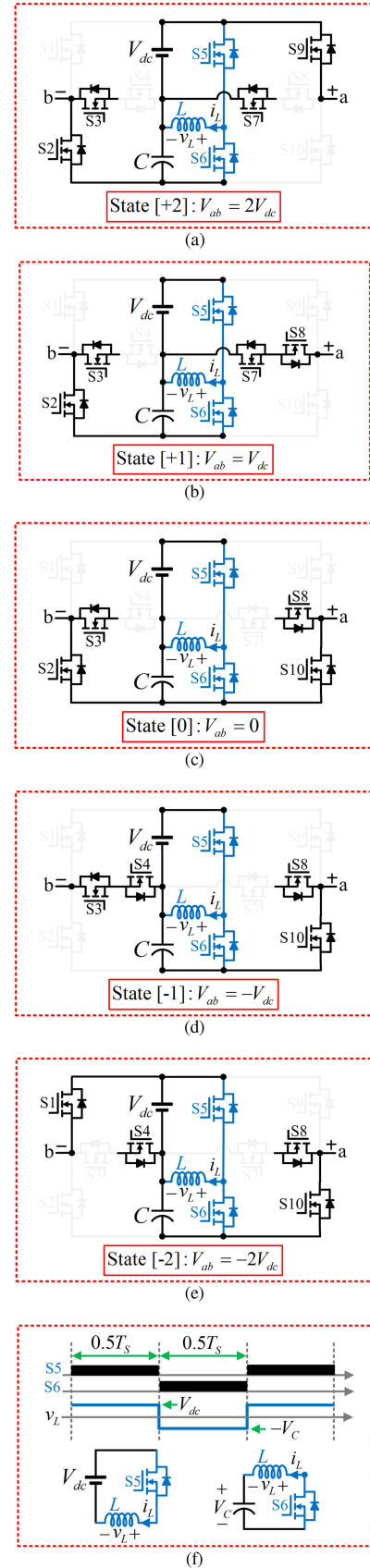


Fig. 4. Switching states of the proposed DTT-5L-CMI: (a) state [+2], (b) state [+1], (c) state [0], (d) state [-1], (e) state [-2], and (f) soft charging of  $C$ .

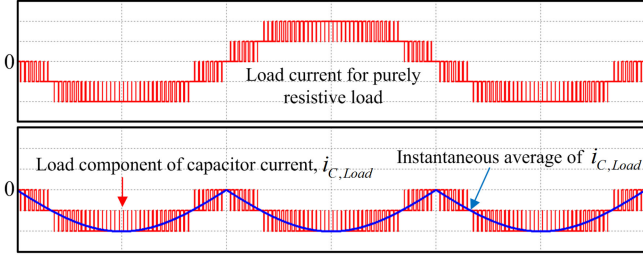


Fig. 5. Load component of capacitor current.

$R_{Load}$  indicates the load resistance. Assuming the capacitor voltage is constant at  $V_{dc}$ , the average power flowing out of the capacitor is

$$P_{C,out} = \frac{4MV_{dc}^2}{\pi R_{Load}}. \quad (3)$$

The output power of the proposed topology considering the fundamental component of load current in Fig. 5 is

$$P_{out} = \frac{2M^2V_{dc}^2}{R_{Load}}. \quad (4)$$

The input power is

$$P_{in} = I_{dc}V_{dc} \quad (5)$$

where  $I_{dc}$  is the average input current. Taking the ratio of (3) to (4), the proportion of total inverter power flowing through capacitor  $C$  is given as

$$\frac{P_{C,out}}{P_{out}} = \frac{2}{\pi M}. \quad (6)$$

Noticed that the maximum proportion of power flowing through capacitor  $C$  is limited to unity when  $M$  is less than 0.63. Therefore

$$\frac{P_{C,in}}{P_{in}} = \begin{cases} 1, & 0 < M < 0.63 \\ \frac{2}{\pi M}, & 0.63 < M < 1. \end{cases} \quad (7)$$

The average inductor current is obtained by substituting (2) and (5) into (7)

$$I_L = \begin{cases} 2I_{dc}, & 0 < M < 0.63 \\ \frac{4I_{dc}}{\pi M}, & 0.63 < M < 1. \end{cases} \quad (8)$$

### C. Capacitor Voltage Ripple and Inductor Current Ripple

Voltage ripple of capacitor  $C$  and current ripple of inductor  $L$  are analyzed in this section. These ripples consist of high-frequency component due to pulsewidth modulation (PWM) switching operation and low-frequency component at double fundamental frequency due to power pulsation of single-phase system. Therefore, the ripples are written as

$$\Delta V_C = \Delta V_{C,LF} + \Delta V_{C,HF} \quad (9)$$

$$\Delta I_L = \Delta I_{L,LF} + \Delta I_{L,HF} \quad (10)$$

where  $\Delta V_C$ ,  $\Delta V_{C,LF}$ , and  $\Delta V_{C,HF}$  represent the total capacitor voltage ripple, low-frequency capacitor voltage ripple, and high-frequency capacitor voltage ripple, respectively, while  $\Delta I_L$ ,  $\Delta I_{L,LF}$ , and  $\Delta I_{L,HF}$  represent the total inductor

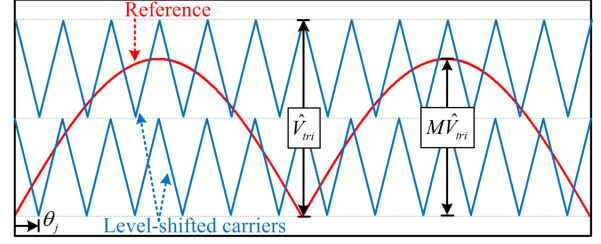


Fig. 6. Modulation scheme for each module.

current ripple, low-frequency inductor current ripple, and high-frequency inductor current ripple, respectively. Considering the volt-second balance of the inductor and charge balance of capacitor during steady state with a constant PWM duty cycle of 0.5, the high-frequency ripples can be obtained as

$$\Delta V_{C,HF} = \frac{I_{dc}}{4Cf_s} \quad (11)$$

$$\Delta I_{L,HF} = \frac{V_{dc}}{2Lf_s} \quad (12)$$

where  $f_s$  is the switching frequency, and  $I_{dc}$  is the average input current.

To derive the low-frequency ripple, the load component of capacitor current,  $i_{C,Load}$ , depicted in Fig. 5, is considered. By performing Fourier decomposition on the waveform described by the instantaneous average of  $i_{C,Load}$ , the peak of double fundamental frequency current flowing through the capacitor is

$$\hat{I}_{C,2f_o} = \frac{8MV_{dc}}{3\pi R_{Load}} \quad (13)$$

where  $M$  depicts modulation index,  $R_{Load}$  denotes the load resistor,  $f_o$  denotes the fundamental output frequency, and  $\hat{I}_{C,2f_o}$  denotes the peak of double fundamental frequency current. The low-frequency capacitor voltage ripple is the peak-to-peak voltage at double fundamental frequency

$$\Delta V_{C,LF} = \frac{4MV_{dc}}{3\pi^2 f_o^2 C R_{Load}}. \quad (14)$$

The voltage across inductor at double fundamental frequency is considered to obtain the low-frequency inductor current ripple

$$\Delta I_{L,LF} = \frac{MV_{dc}}{6\pi^3 f_o^2 L C R_{Load}}. \quad (15)$$

In overall, the ripples of capacitor voltage and inductor current are written as

$$\Delta V_C = \frac{4MV_{dc}}{3\pi^2 f_o^2 C R_{Load}} + \frac{I_{dc}}{4Cf_s} \quad (16)$$

$$\Delta I_L = \frac{MV_{dc}}{6\pi^3 f_o^2 L C R_{Load}} + \frac{V_{dc}}{2Lf_s}. \quad (17)$$

### D. Modulation Scheme and Cascaded Extension

The proposed DTT-5L-CMI can be extended by cascading multiple modules to increase the levels and voltage generation. Fig. 6 shows that two level-shifted carriers are required for each module. With  $n$  cascaded modules, the phase angle of carriers



for  $j$ th module is

$$\theta_j = \frac{360^\circ}{n} (j - 1). \quad (18)$$

The output fundamental peak voltage is

$$\hat{V}_{o,1} = MV_{\max} \quad (19)$$

where  $M$  denotes the modulation index defined by the ratio of reference sine wave peak to the total peak-to-peak of level-shifted triangular carriers, as depicted in Fig. 6, and  $V_{\max}$  denotes the maximum voltage level,  $V_{\max} = 2nV_{dc}$ . The maximum number of voltage levels generation with  $n$  cascaded modules is

$$N = 4n + 1. \quad (20)$$

#### E. Comparison With Other Topologies

The SC-CMI has recently arisen as an emerging topology where various configurations are reported in literatures. However, the current spike issue induced from capacitor charging process is rarely discussed. In [21], an inductor inserted in between dc source and SC is used to charge the capacitor without current spike. The switching states are designed to synthesize a staircase ac voltage with precomputed duty cycle and switching angle. Unfortunately, the inductor has to be controlled at frequency of only double of that in output voltage, making it not appropriate for power frequency (50/60 Hz) applications. High output frequency of 25 kHz is implemented in [21].

Alternatively, a new SC topology based on CHBs together with a charging circuit consists of an inductor, one diode for each H-bridge, and a switch is proposed in [22]. The capacitor is charged from dc source through a series inductor with antiparallel diode to cater for current spike issue. Utilization of antiparallel diode is dedicated to prevent the capacitor from overcharging and voltage spike occurrence. It provides a freewheeling current path after the capacitor voltage reaches the dc source voltage. This also signifies that the inductor current freewheels through the diode and dissipates power. Special consideration has also been made to avoid continuous increase in inductor current. Discontinuous inductor current is achieved by dissipating the inductor energy during freewheeling mode so that the current falls to zero before the commencement of the next charging cycle.

However, it is worth to emphasize that there is a compromise between the inductor size and capacitor charging speed, despite not deeply discussed. The design/derivation of the inductor value and the corresponding capacitor charging current are not presented. Small inductance value is usually considered in this topology owing to the short capacitor charging period. In this instance, the impulse charging current might not be effectively eradicated, as evidenced by the visible impulse current in the presented experimental results [22]. Additionally, the level-shifted sinusoidal pulse width modulation (SPWM) that is deemed to be the most suitable switching technique for this topology results in the undesirable nonuniform operation among H-bridges. Some experimental evidences from [22] clearly demonstrate uneven capacitor voltage waveform with different ripple magnitude, charging period, and discharging period. It should be emphasized that other switching techniques are less appropriate in this topology due to the restricted capacitor charging pattern, as mentioned in [22].

TABLE I  
COMPARISON BETWEEN THE PROPOSED DTT-5L-CMI AND OTHER FIVE-LEVEL SC-CMI TOPOLOGIES

	(a)	(b)	(c)	(d)	(e)	(f)
[15]	6	1	1	0	no	no
[22]	9	3	2	1	partially	no
[23]	7	4	2	0	no	no
[24]	13	0	2	0	no	no
Proposed DTT-5L-CMI	10	0	1	1	yes	yes

Note: (a) Number of switches. (b) Number of diodes. (c) Number of capacitors. (d) Number of inductors. (e) Soft charging for capacitor. (f) Uniform operation for cascaded extensions.

The proposed DTT-5L-CMI resolved the current spike issues without compromising the uniform operation of the CMI. For clarity, a comparison of the proposed DTT-5L-CMI and some recently presented five-level SC-CMI topologies is summarized in Table I. At first glance, the proposed topology requires a moderate number of components count among all. However, in the practical implementation for SC-CMI topologies in [15], [23] and [24], it is always essential to precharge their SCs to the steady-state voltage prior to turning on the inverter system. In this regard, short circuit across the dc source can be prevented. However, additional switches in precharging circuit are not considered in these references, and therefore they have higher switch implementation requirement. The proposed topology eliminates the need of precharging circuit and it can be conveniently employed for practical applications. Besides, it exhibits a significant advantage over other SC-CMI topologies by ensuring continuous charging of capacitor from dc source, while simultaneously supplying the loads.

The proposed DTT-5L-CMI resolves the current spike issue of all the contemporary five-level SC-CMIs with improved reliability. With only two additional switches, the voltage gain is enhanced to double as compared to a conventional five-level CHB. In addition, the number of dc sources is also reduced by half. This indicates that half of the converters required for dc voltage generation as in a CHB can be eliminated in the proposed topology. While the voltage boosting characteristic of the proposed topology enables single-stage dc-ac power conversion, the dc-dc boost converter can be omitted for improved system efficiency and reliability, which renders it particularly suitable for renewable energy systems with low input voltage.

#### IV. SIMULATION RESULTS

Simulations were conducted to study the feasibility of the proposed topology. Two cascaded modules ( $n = 2$ ) with dc sources voltage of 100 V each are considered. The simulation results are depicted in Fig. 7. Each module is generating five symmetrical voltage levels between  $-200$  and  $200$  V. Their maximum voltage level is twice of the dc source voltage, thus validating a voltage gain of two. A total of nine distinct voltage levels are generated and the maximum voltage level is extended to 400 V.

Individual module is also investigated in this simulation. Observations shows that the capacitor voltage, capacitor current, and inductor current captured for both modules are similar. This implies that the operations for both modules are uniform and the modularity feature of cascaded inverter structure is retained. It is

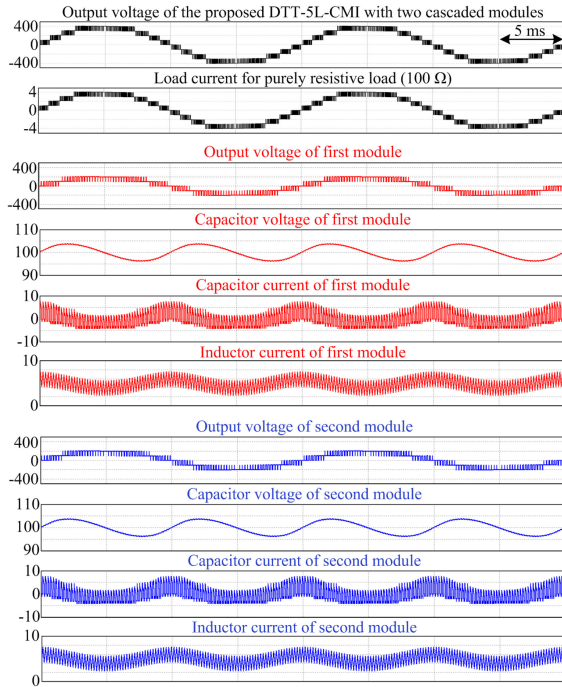


Fig. 7. Simulation results of the proposed DTT-5L-CMI with two cascaded modules ( $n = 2$ ).

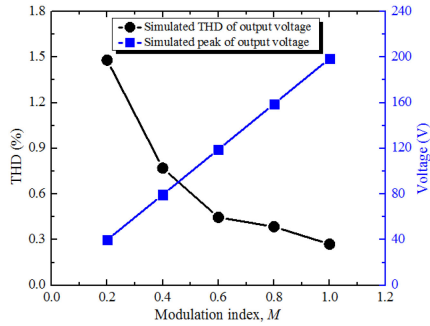


Fig. 8. Simulated THD and peak of output voltage ( $n = 1$ ).

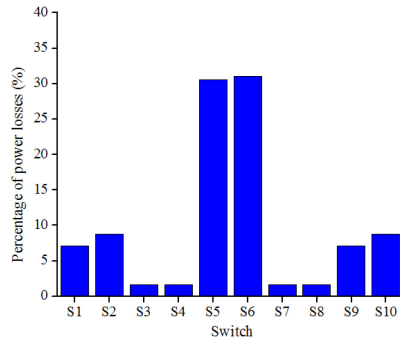


Fig. 9. Simulated power losses distribution for  $M = 1$  ( $n = 1$ ).

also demonstrated in Fig. 7 that the capacitor charging current is determined by the inductor current. This is because the capacitor in each module is charged through its respective inductor. In this regard, soft switching is achieved and no impulse current is observed in the plotted capacitor current waveforms.

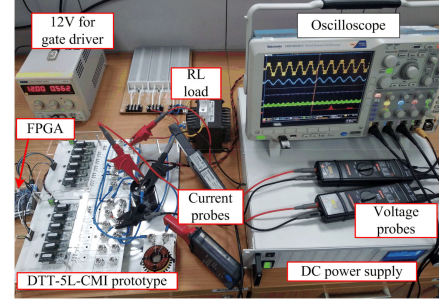


Fig. 10. Experimental setup of the proposed DTT-5L-CMI.

TABLE II  
PROTOTYPE SPECIFICATIONS

Description	Value/Parameter
Input voltage, $V_{dc}$	100 V
Carrier frequency	5 kHz
Capacitor, $C$	1000 $\mu$ F
Inductor, $L$	3 mH
Load resistor	100 $\Omega$
Load inductor	0.1 H

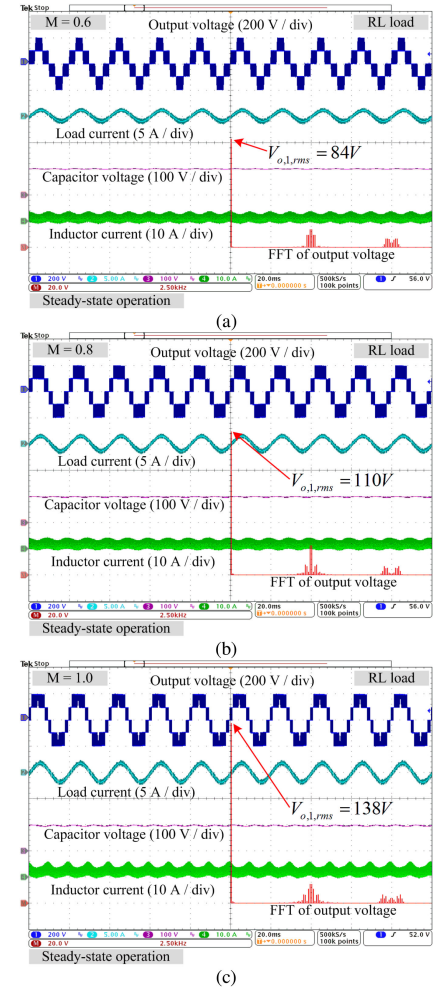


Fig. 11. Steady-state waveforms of the proposed DTT-5L-CMI with RL load. (a)  $M = 0.6$ . (b)  $M = 0.8$ . (c)  $M = 1.0$ .

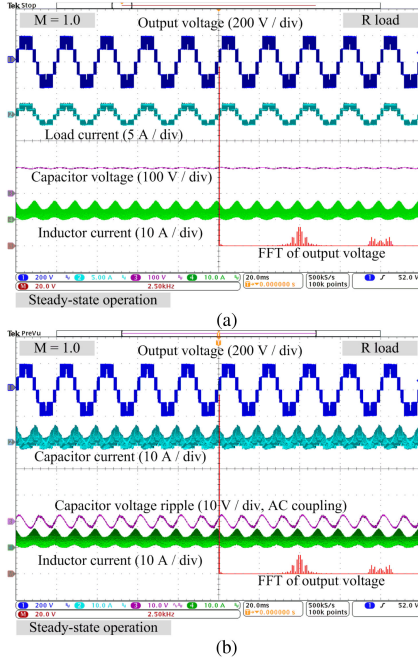


Fig. 12. Steady-state waveforms of the proposed DTT-5L-CMI with purely resistive load and  $M = 1.0$ .

Simulation was continued to study the performance of the proposed topology when practical power switches are taken into consideration. Power MOSFETs used in the experimental prototype were modeled accurately in PSIM software. Thermal module is used to perform curve fitting for the characteristic graphs specified in the datasheet. Using the same parameters as those in the experimental prototype, the simulated output voltage that is supplying purely resistive load for different modulation indexes are analyzed and illustrated in Fig. 8. With single module ( $n = 1$ ), it is clear that the maximum voltage level is twice of the input dc source, that is 200 V. It is also validated that the peak of output voltage for different  $M$  shows good agreement with (19), with the simulated values slightly less than the calculated values. Besides, the total harmonic distortion (THD) of the output voltage is noted to be decreasing with  $M$ , while the maximum THD at  $M = 0.2$  is as low as 1.5%.

A power losses analysis was then conducted at  $M = 1$  where the simulated efficiency is approximately 99%. Fig. 9 shows the power losses distribution among the ten switches. Note that the power losses of two switches in each half bridge (S1–S2, S5–S6, and S9–S10) are almost balanced. Therefore, the proposed topology can also be implemented by using three half bridge modules with four additional switches.

## V. EXPERIMENTAL RESULTS

For further validation, an experimental prototype was implemented and tested. Fast Fourier transform function of the oscilloscope was used to compute the fundamental component of the output voltage. The experimental setup and its corresponding specifications can be found in Fig. 10 and Table II, respectively. Fig. 11 shows the measured steady-state waveforms under inductive load. The load current is sinusoidal and the average capacitor voltage is 100 V for all modulation indexes.

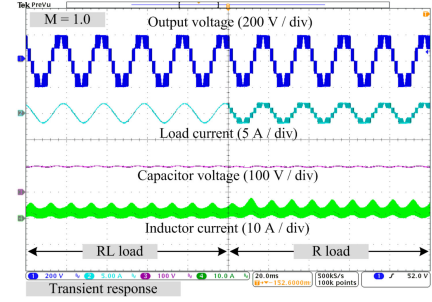


Fig. 13. Transient response of the proposed DTT-5L-CMI from  $RL$  load to  $R$  load.

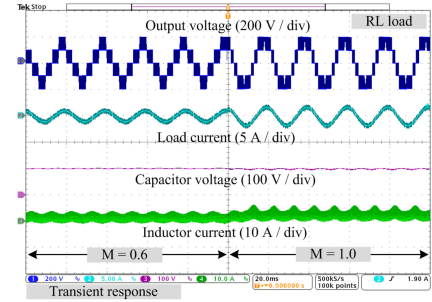


Fig. 14. Transient response of the proposed DTT-5L-CMI from  $M = 0.6$  to  $M = 1.0$ .

Five voltage levels are generated between  $-200$  and  $200$  V. It is clear that the magnitude of the fundamental output voltage is proportional to the modulation index with the measured value slightly less than the theoretical calculation using (19).

Experimental tests are then continued with purely resistive load, as shown in Fig. 12(a). The load current is proportional to the voltage with five distinctive levels are observed. Fig. 12(b) demonstrates the corresponding plots when the oscilloscope channel was set to ac coupling. The measured capacitor voltage and current shows very good agreement with those obtained in simulation, thus further providing a proof of the operation and viability of the proposed topology.

Transient response of the experimental prototype was also conducted. In Fig. 13, smooth transition in load current is observed when the load is switched from  $RL$  to purely resistive load. The step change in modulation index from 0.6 to 1.0 in Fig. 14 clearly shows that the magnitude of the load current increases instantaneously without affecting the average capacitor voltage.

## VI. CONCLUSION

In this article, a novel CMI topology is presented. Theoretical analyses were conducted and validated by simulation and experimental study of a prototype. The proposed DTT-5L-CMI is capable of five levels generation with double voltage boosting gain. Soft charging of capacitor and uniform operation for all cascaded modules are achieved that resolved the problems of recent SC-CMI. Therefore, the proposed topology is an attractive alternative for dc-ac power conversion system.

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